REMARKS

The subject Office Action objected to claim 6 for claiming an additional method step which is allegedly inherent in the already claimed process. Claim 6 is rejected under 35 USC §112 for allegedly being broader than the specification describes. Claims 1 – 6 and 8 were rejected under 35 USC §103 as being unpatentable over US Patent No. 5,087,322 to Lillienfeld et al. in combination with No. 5,635,412 to Baliga et al. Claim 7 was rejected under 35 USC §103 as being unpatentable over US Patent No. 5,087,322 to Lillienfeld et al. in combination with No. 5,635,412 to Baliga et al. and further in view of No. 5,612,232 to Thero et al. As amended hereby, the claims are clarified and amended to more precisely define the invention, thus it is respectfully submitted that claims 1 – 8 are now in condition for allowance, as are new claims 18 – 20.

In response to the objection and §112 rejection, claim 6 is amended hereby to include an additional limitation defining the "treatment" as being "selected from a group consisting of chemical cleaning, surface etching and ion implantation." This limiting language is found in the application at page 5, 2nd full paragraph.The objection and Sec. 112 rejection are thus believed to be overcome.

With respect to claims 1 – 8, the present invention is for an apparatus and method of making a Schottky barrier semiconductor device that is different from any device disclosed in the known prior art. As clearly delineated in the application from page 5, 1st full paragraph through page 7, top pargraph, the sequence of process steps defined in the amended claims is believed to be distinctive over the cited prior art. As indicated in

claim 1, which is amended to incorporate the limitations of cancelled claim 2, the process involves the following sequential steps:

a) forming an insulating layer,
b) placing a mask on the insulating layer,
c) etching away a portion of the insulating layer,
d) retaining the mask in place and depositing conductive material on the wafer surface,
e) stripping off the mask, and
f) implanting an edge termination layer.

By way of contrast, the cited patent to Lillienfeld et al. shows 2 embodiments. The first process described by Lillienfeld in figures 1A – 1D involves the following step sequence, not involving an insulating layer:

1. placing a mask on the semiconductor,
2. modifying the semiconductor surface,
3. depositing conductive material on the wafer surface, and
4. stripping off the mask.

The second Lillienfeld process of figures 2A – 2g provides for an insulating layer, but then removes the mask before the CVD step:

a) forming an insulating layer,
b) placing a mask on the insulating layer,
c) etching away a portion of the insulating layer,
d) modifying the semiconductor surface, ~ optional step
e) stripping off the mask,
g) depositing conductive material on the wafer surface, and
f) removing the insulating layer.

In other words, the first disclosed Lillienfeld process fails to combine an insulating layer with a mask, and the second process, while initially utilizing an insulating layer and a mask, removes the mask prior to the step of depositing conductive material. Thus both

the Lillienfeld methods are different from the process of the present invention. As seen in Figures 2D and 2E in the present application and described from the paragraph beginning at the bottom of page 5 through the full paragraph in the middle of page 6, "maintaining the mask in place" optimizes the clear definition of the edges of Schottky contacts 30b and 30d. By allowing portions of CVD material to be deposited upon the mask, and forming the conductive layer thinner than the mask, the conductive material settles cleanly into the trench created in the insulating material and the surplus conductive material is cleanly removed with the mask. An unreconciled drawback of the Lillienfeld disclosure is that the conductive material deposited onto the wafer surface within an opening in the insulating layer is that of achieving sharp edges to separate the conductive region from the substrate.

Furthermore, it is established practice in the process of drafting method claims to recite the steps in logical, or necessary, order (see, e.g., Mechanics Of Patent Claim Drafting, John L. Landis, Practicing Law Institute, Section 35). The order of steps described by Lillienfeld differs from that of the invention according to amended claim 1 by removing the mask before depositing the conductive material.

As such, the major steps of the present invention are believed to distinguish patentably over the Lillienfeld teaching, thus also avoiding the Baliga reference regarding the edge termination limitation as moot. Claim 1 as amended is believed to be allowable. Claims 3 – 8, being dependent from amended claim 1, are also believed to be allowable.

In a further embodiment of the invention, new claims 18 – 20 make the edge

termination implantation an optional step, as is stated in the paragraph straddling page 6 – page 7. Claims 18 – 20 also distinguish over the prior art, as discussed above. Therefore, it is respectfully submitted that new claims 18 – 20 are allowable.

A marked-up copy of amended claims 1 and 6, showing the changes, is appended hereto.

The amendment to the specification is made to correct a minor typographical error.

In view of the foregoing amendment and remarks, it is respectfully submitted that all claims pending are allowable. Therefore, reconsideration and allowance are respectfully requested.

Respectfully submitted,

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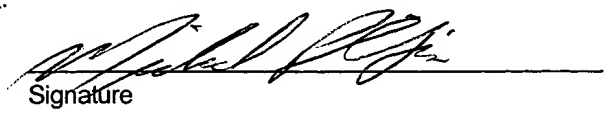

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MARKED UP VERSION SHOWING THE CHANGE TO THE SPECIFICATION

Page 3:

A Schottky barrier diode is illustrated in Figure 1 that is formed according to the process of prior filed patent application No. 09/700,627, incorporated herein by reference. Ohmic contact layer 18, for example having metal contacts, and preferably formed of titanium, and Schottky rectifying contact 14 are deposited on and bonded to a SiC wafer 10. An ion implanted edge termination region 16 is created in SiC wafer 10 adjacent the edges of Schottky contact 14, preferably using an inert gas ion, for example argon. A low temperature oxide passivated layer 12 is then deposited on [water] **wafer** 10 adjacent Schottky contact 14. While it is believed that the Schottky barrier diode so fabricated has the requisite properties to function as required, the manufacturing process involves three lithographic masking steps to form contact 14, oxide layer 12, and edge termination 16 requiring the use of state-of-the-art equipment. The second and third mask applications require two alignment steps, and this method is thus time consuming and expensive.

MARKED UP VERSION SHOWING CHANGES TO CLAIMS 1, 3, 5 and 6:

1. (Amended) A method for the fabrication of a Schottky barrier diode on a SiC wafer, comprising the steps of:

(a) **forming an insulating layer on the surface of the SiC wafer**;

(b) placing a mask having a window on an exposed surface of the [SiC wafer] **insulating layer**;

(c) **etching away a portion of the insulating layer corresponding to the window to expose a portion of the SiC wafer therebeneath**;

(d) **while retaining the mask in place,** depositing conductive material on the mask and exposed portions of the wafer surface;

(e) stripping off the mask so as to leave the conductive material deposited upon the portion[s] of the wafer surface **corresponding to the window**; and

(f) implanting an edge termination layer **in**to the wafer beneath the surface thereof but not beneath the conductive material.

3. (Amended) The method for the fabrication of a Schottky barrier diode as described in claim [2] **1**, wherein the step of forming an insulating layer comprises forming an oxide layer.

5. (Amended) The method for the fabrication of a Schottky barrier diode as described in claim 4, wherein the inert ion**s** comprise**[s]** argon ions.

6. (Amended) The method for the fabrication of a Schottky barrier diode as described in claim [2] 1, further comprising the step of applying a treatment to the exposed portion of the SiC wafer surface, **the treatment selected from a group consisting of chemical cleaning, surface etching and ion implantation**.